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ENHANCED PLANARIZATION TECHNIQUE FOR AN INTEGRATED CIRCUIT

This application is a continuation of patent application Ser. No. 08/456,343, filed Jun. 1, 1995 now abandoned which is a continuation of Ser. No. 08/163,043 filed on Dec. 6, 1993 now U.S. Pat. No. 5,435,888.

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates to formation and structures for interlevel dielectrics in integrated circuit fabrication.

A high degree of planarization is essential in the fabrication of integrated circuits with multiple levels of interconnect. Application of spin-on glass,[1] followed by global etch-back, is widely used in the industry to achieve the desired level of surface planarity. However, spin on glass ("SOG") and SOG etch-back technique are inadequate in a variety of situations where topologies with high aspect ratio and/or more topologies are encountered due to lack of planarization and/or sog cracks.

[1]Spin-on glass deposition is an example of a "sol-gel" process, which has been used in the semiconductor industry for many years. The unprocessed spin-on glass material (available in numerous formulations) is a fluid material (actually a gel). After the liquid material is coated onto the face of a wafer, the wafer is rotated at high speed to throw off the excess material. The surface tension and adhesion of the material provides a flat (planarized) surface with a controlled thickness. The liquid material is then baked, to drive off solvents and provide a stable solid silicate glass. See generally, e.g., Dauksher et al., "Three 'low Dt' options for planarizing the pre-metal dielectric on an advanced double poly BiCMOS process," 139 J. Electrochem Soc 532–6 (1992), which is hereby incorporated by reference.

In most cases, successful planarization of severe topologies is achieved by a single or double SOG deposition+etchback step in the following sequence:

a) a layer of dielectric is applied between the underlying surface and SOG.
b) application of a layer of SOG and SOG cure;
c) application of a second layer of SOG and SOG cure (optional); and
d) SOG etchback.

However, in extreme topologies, when the volume of SOG is very large, shrinkage of SOG during planarization and post-planarization processing leads to formation of undesirable cracks or voids.

The proposed method seeks to alleviate the problem of SOG cracking by performing the following operations:

a) Conventional dielectric deposition is applied (optional);
b) Application of a layer of SOG and SOG cure (as in prior art);
c) deposition of a layer of dielectric (e.g. TEOS/ozone deposition, or simple plasma-enhanced-TEOS,[2] or plasma-enhanced-silane oxide) with or without dopant can be used to adjust for etch back selectivity between SOG and dielectric. Thicknesses between 1000 Å to 5000 Å can be used.

[2]"TEOS," or tetraethoxysilane, is a popular and convenient feedstock for deposition of oxides from the vapor phase.

d) application of a second layer of SOG and/or SOG cure: and
e) SOG etchback.

This process will leave a layer of dielectric between the 1st and the 2nd SOG layers in locations where conventional planarization technique are likely to crack or void. This provides enhanced reliability.

The thickness of the first SOG layer can be reduced to avoid any undesired effects, such as field inversion of underlying devices or enhanced hot-carrier injection.[3]

[3]See, e.g., Lifshitz et al., "Hot-carrier aging of the MOS transistor in the presence of spin-on glass as the interlevel dielectric," 12 IEEE Electron Device Letters 140–2 (March 1991), which is hereby incorporated by reference.

A positive sloped valley is produced for second dielectric deposition. The step coverage will be enhanced due to this positive slope.

The structure provided by these steps has improved resistance to cracking, and improved resistance to other undesirable possible effects of thick spin-on glass layers.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure; applying and curing spin-on glass, to form a first dielectric; depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer; applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers; performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure; deposition of an interlevel dielectric; etching holes in said interlevel dielectric in predetermined locations; and depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure; applying and curing spin-on glass, to form a first dielectric; depositing silicon dioxide under vacuum conditions, to form a second dielectric layer over said first layer; applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers; performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure; deposition of an interlevel dielectric; etching holes in said interlevel dielectric in predetermined locations; and depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure; applying and curing spin-on glass, to form a first dielectric layer; depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer, said second dielectric layer having a thickness equal to or less than said first layer; applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers, said third dielectric layer having a thickness equal to or greater than said second layer; performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure; deposition of an interlevel dielectric; etching holes in said interlevel dielectric in predetermined locations; and depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

According to a disclosed class of innovative embodiments, there is provided: An integrated circuit, comprising: an active device structure, including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and a planarization structure, overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric; an interlevel

dielectric overlying said planarization structure and said active device structure, and having via holes therein which extend to selected locations of said uppermost conductor layer; and an additional thin-film patterned conductor layer which overlies said interlevel dielectric and extends through said via holes to said selectred locations of said uppermost conductor layer.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

FIGS. 1A–1C show steps in a conventional process;

FIGS. 2A–2C show steps in a first embodiment of the invention;

FIGS. 3A–3C show steps in a second embodiment of the invention.

FIG. 4 shows a sample device structure incorporating a planarization layer according to the disclosed innovations.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

The disclosed process steps can be applied, for example, after fabrication of the first metal layer. Thus, the starting structure would be patterned metallization lines running over an interlevel dielectric which includes contact holes, and also has topographical excursions due to the underlying polysilicon layer(s) and field oxide layer. The maximum topographical excursion will include contributions from all of these. (However, the disclosed innovations can also be applied after fabrication of the second metal layer, before deposition of a third metal layer.)

FIGS. 1A–1C show steps in a conventional process. The starting structure will of course be defined by the previous process steps; but assume, for example, that the recesses have widths of 0.8 μm each, are spaced on a minimum pitch of 1.6 μm, and have a maximum depth of 1 μm. (Of course, these numbers are merely illustrative.)

As shown in FIG. 1A, a first layer 1 of SOG would be spun on and cured, to a thickness of e.g. 3000 Å in flat areas. (The thickness is substantially more in recessed areas) As is well known to those of ordinary skill, the thickness of the SOG is determined by the individual composition and by the spin rate. As seen in FIG. 1A, a single deposition of SOG is not enough to fill the recesses.

As shown in FIG. 1B, a second layer 2 of SOG would then be spun on and cured, to provide an additional thickness of e.g. 3000 Å in flat areas.

A global etchback step is then performed, to remove the SOG from flat areas. The resulting surface contour, as shown in FIG. 1C, is susceptible to cracking.

FIGS. 2A–2C show steps in a first embodiment of the invention. Assume that the same recess dimensions are used as in FIGS. **1A–1C**. Again, the specific dimensions and parameters given here are merely illustrative, and do not delimit the invention.

A first layer **1** of SOG is deposited as in FIG. **1A**. That is, for example, a siloxane-based spin-on glass[4] is spun on to a thickness of 2000 Å over flat areas, and is then cured for 60 minutes at 425° C.

[4]Such materials may be obtained, for example, from Ohka America™ or Allied Signal™ or other suppliers.

A layer **3** of low-temperature oxide is then deposited, to a thickness of 2000 Å. (For example, this may be done by plasma-enhanced deposition of TEOS.) This produces the structure shown in FIG. 2B.

A second layer **2** of SOG is then be spun on and cured, to provide an additional thickness of e.g. 3000 Å in flat areas.

A global etchback step is then performed, to remove the SOG and TEOS from flat areas. The resulting surface contour, as shown in FIG. 2C, provides improved filling of the recessed areas. Moreover, the combination of slightly different materials (SOG and low-temperature oxide) reduces susceptibility to cracking.

For simplicity, the drawing of FIG. 2C shows exactly 100% etchback, but of course the degree of etchback can be varied if desired.

FIGS. **3A–3C** show steps in a second embodiment of the invention. This may be particularly advantageous with more extreme topologies. In this embodiment, assume, for example, that the recessed areas have widths of 0.8 μm each, are spaced on a minimum pitch of 1.6 μm, and have a maximum depth of 2 μm. (Of course, these numbers are merely illustrative.)

A first layer **1** of SOG is spun on and cured to produce a thickness of 2000 Å over flat areas, as shown in FIG. **3A**.

A layer **3** of low-temperature oxide is then deposited, to a thickness of 3000 Å. (For example, this may be done by plasma-enhanced deposition of TEOS.) This produces the structure shown in FIG. **3B**.

A second layer **2** of SOG is then be spun on and cured, to provide an additional thickness of e.g. 2000 Å in flat areas.

A global etchback step is then performed, to remove the SOG and TEOS from flat areas. The resulting surface contour, as shown in FIG. 3C, provides improved filling of the recessed areas, even under extreme topologies. Moreover, the combination of slightly different materials (SOG and low-temperature oxide) reduces susceptibility to cracking.

For simplicity, the drawing of FIG. **3C** shows exactly 100% etchback, but of course the degree of etchback can be varied if desired.

In alternative embodiments, it is also possible to deposit a plasma oxide before the first layer of spin-on glass. (This is commonly done to prevent direct contact between the SOG and the underlying metallization.) In this embodiment, 1000 Å–5000 Å of (for example) TEOS oxide would be deposited before the first layer of SOG.

Processing then continues with deposition of an interlevel dielectric, such as PSG, and conventional further processing steps.

One particular advantage of the disclosed invention is that it can be very easily implemented (in at least some processes) by a simple transposition of steps (depositing the low-temperature oxide before, rather than after, the second layer of spin-on glass).

FIG. **4** shows a sample device structure incorporating a planarization layer according to the disclosed innovations. In this example, the partially fabricated device structure included active devices **12** in a substrate **10**, including polysilicon lines **14**. Field oxide **13** provides lateral separa-